IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: W. Mintel	
Serial No.:	08/903,486	Group Art Unit: 2811	
Filed:	July 29, 1997	Docket: 303.326US1	
Title:	SILICON CARBIDE GATE TRANSISTOR		

#26
5/1/01
P. Vasudevan

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated 21 December 2000, please amend the above-identified patent application as follows.

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the Office action, thereby moving the deadline for response from 21 March 2001 to 21 April 2001.

IN THE CLAIMS

Please substitute the attached claim set entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows and add claims 55-57:

1.(Three Times Amended) A [transistor] system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is less than 0.5, the gate being connected to receive an input signal[.];

addressing circuitry to address memory cells in the array; and

control circuitry to control read, write, and erase operations of the memory device.